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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,445	07/18/2003	Yasuo Yamagishi	030868	1112

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EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 04/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/621,445	YAMAGISHI ET AL.
	Examiner	Art Unit
	Jermele M. Hollington	2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,6,7,10 and 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10 and 11* is/are allowed.

6)☒ Claim(s) *1-2, 4 and 6-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-2, 4 and 6-7 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eldridge et al (6727579).

Regarding claim 1, Eldridge et al disclose [see Fig. 33] a probe card (carrier assembly 3300) for testing a semiconductor chip (electronic component 3302) comprising: plurality of probes (resilient contact structure 3322); build-up interconnection layer (multi-layer substrate

3320) having a multilayer interconnection structure therein, said interconnection structure comprising plural interconnection layers [not number but shown] and one or more resin insulation layers (3320a) insulating said interconnection layers from each other, said build-up interconnection layer (3320) carrying said plurality of probes (3322) on a top surface thereof in electrical connection with said multilayer interconnection structure; and a decoupling capacitor (decoupling capacitor 3370) embedded resin insulation layer (3320a) constituting said build-up interconnection layer (3320) in electrical connection with one of said probes (3322) via said multilayer interconnection structure (3320), said multilayer interconnection structure (3320) including an inner via-contact (contact pads 3324) in the vicinity of said probe (3322). However, they do not disclose a decoupling capacitor completely covered on its top surface by a resin insulation layer. It is well known to completely covered the decoupling capacitor where needed (see MPEP 2144.04; In re Seid, 161 F.2d 229, 73 USPQ 431 (CCPA 1947)). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the insulation layer to cover the decoupling since covering the capacitor would be aesthetic design change relating to ornamentation. The court held that matters relating to ornamentation only which have no mechanical function cannot be relied upon to patentably distinguish the claimed invention from the prior art.

Regarding claim 2, Eldridge et al disclose said capacitor (3370) has a thickness generally equal to or less than a thickness of said resin insulation layer (3320).

Regarding claim 4, Eldridge et al disclose said capacitor (3370) is formed in said build-up interconnection layer (3320) right underneath one of said probes (3322).

5. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eldridge et al (6727579) in view of Fukuzumi et al (6548844).

Regarding claim 6, Eldridge et al disclose [see Fig. 33] a probe card (3300) for testing a semiconductor chip (3302), comprising: a capacitor (3370) embedded resin insulation layer (3320a) constituting said build-up interconnection layer (3320) in electrical connection with one of said probes (3322) via said multilayer interconnection structure (3320). However, they do not disclose the feature of the capacitor as claimed. Fukuzumi et al disclose [Fig. 1] a capacitor structure 1 includes a dielectric film (capacitor dielectric film 3) of a complex oxide containing at least one metal element selected from the group consisting of Sr, Ba, Pb, Zr, Mg and Nb [see col. 5, lines 25-38]. Further, Fukuzumi et al teach that the addition of features of the capacitor is advantageous because it suppresses the deterioration of the data retaining characteristic that is originated from when annealing is performed in an atmosphere containing a reduce agent. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Horel et al by adding the features of the capacitor as taught by Fukuzumi et al in order to suppress the deterioration of the data retaining characteristic that is originated from when annealing is performed in an atmosphere containing a reduce agent.

Regarding claim 7, Eldridge et al disclose [see Fig. 33] a probe card (3300) for testing a semiconductor chip (3302), comprising: a capacitor (3370) embedded resin insulation layer (3320a) constituting said build-up interconnection layer (3320) in electrical connection with one of said probes (3322) via said multilayer interconnection structure (3320). However, they do not disclose the feature of the capacitor as claimed. Fukuzumi et al disclose [Fig. 1] a capacitor structure 1 includes an upper (common electrode 4) and lower (dispersion electrode 2) electrodes

sandwiching a dielectric film (capacitor dielectric film 3), said upper (4) and lower (2) electrodes containing at least one metal element or a metal oxide selected from the group consisting of Pt, Au, Cu, Pb, Ru, a Ru oxide, Ir, an Ir oxide, and Cr [see col. 5, lines 43-45 and col. 6, lines 8-25]. Further, Fukuzumi et al teach that the addition of features of the capacitor is advantageous because it suppresses the deterioration of the data retaining characteristic that is originated from when annealing is performed in an atmosphere containing a reduce agent. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Horel et al by adding the features of the capacitor as taught by Fukuzumi et al in order to suppress the deterioration of the data retaining characteristic that is originated from when annealing is performed in an atmosphere containing a reduce agent.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892 for details.

7. Applicant's arguments filed Jan 27, 2006 have been fully considered but they are not fully persuasive.

a) The applicants argue: *"Thus, FIG. 33 clearly shows that decoupling capacitor 3370 is not entirely embedded in substrate 3320 because it is not covered on its top surface by the substrate, in contrast to the present invention, in which embedded capacitor 20 is entirely covered on its top surface by the build-up interconnection layer 14, as shown in FIG. 4."*

In response to the above arguments, although it appears that Eldridge et al may not cover capacitor 3370, the prior art still uses the probe card (assembly 300) structure for testing a semiconductor device (electronic component 3302) as claimed. The examiner does not see any

difference of using the capacitor with the cover insulation layer. Eldridge et al have established that covering the capacitor would not beneficial when testing the semiconductor device. In col.113, lines 5-19, it states; " As mentioned hereinabove, the ability to include a decoupling capacitor (or a plurality of decoupling capacitors) in an assembly is often a very important consideration affecting the performance envelope of certain electronic components, such as microprocessors. **Generally (i.e., as a rule of thumb), the shorter the path from a semiconductor device to a decoupling capacitor, the better (e.g., the lower its inductance).** The assembly shown herein provides a very short path, and consequent low inductance coupling, between an electronic component (3302) such as a high-speed microprocessor and a printed circuit board (3320)..."

b) The applicants further argue: *"More specifically, in FIG. 33, the capacitor is provided in a depression formed in a build-up substrate and there is formed a gap between the capacitor and the sidewall or bottom surface of the depression, in which the capacitor is provided. Thus, the capacitor of Eldridge et al. is not enclosed or surrounded "closely" in contrast to the meaning of the word "embed." According to Webster's New World Dictionary Third College Edition, "embed" means to "set or fix firmly in a surrounding mass." Clearly, the capacitor of Eldridge et al. is not set or fixed firmly in a surrounding mass. Thus, contrary to the disclosure of Eldridge et al., the capacitor of the present invention fully meets the dictionary definition of "embedded."*

In response to the above argument, the examiner has to disagree with the arguments. In reviewing the Eldridge et al, the examiner believes the capacitor 3370 is set firmly around multi-layer substrate 3320. The applicants are correct that there is a gap between the substrate and capacitor but that does not mean that it is not firmly set. Base on the definition given by the applicants, the examiner is taking the position that a device could be surrounded by a mass but it does not means that it is connected to that mass from all sides.

Therefore the examiner believes that the prior art still reads on the claimed invention.

8. Claims 10-11 are allowed over the prior art.

9. The following is a statement of reasons for the indication of allowable subject matter: regarding claim 10, the primary reason for the allowance of the claim is due to the specific limitation of a test method of a semiconductor device comprising the step of before contacting said probe card to said semiconductor chip, of setting an impedance between said probe and said capacitor to be substantially equal to an impedance of a semiconductor package including therein said semiconductor chip and a capacitor, for a part between said semiconductor chip and said capacitor. Since claim 11 depends from claim 10, it is also have allowable subject matter.

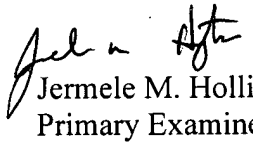
10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (517) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jermele M. Hollington
Primary Examiner
Art Unit 2829

JMH
April 17, 2006